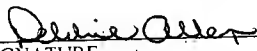


Client Reference No. 068758.0139

PATENT

CERTIFICATE OF MAILING VIA FIRST CLASS MAIL	
PURSUANT TO 37 C.F.R. § 1.8, I HEREBY CERTIFY THAT I HAVE INFORMATION AND A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE WILL BE DEPOSITED AS FIRST CLASS MAIL WITH THE UNITED STATES POSTAL SERVICE IN AN ENVELOPE ADDRESSED TO:	
MAIL STOP PATENT APPLICATION COMMISSIONER FOR PATENTS P.O. BOX 1450 ALEXANDRIA, VA 22313-1450	
 SIGNATURE	OCTOBER 31, 2003 DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ted Johansson

Serial No.:

Filing Date: October 31, 2003

Title: Semiconductor Process and Integrated Circuit

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Group Art Unit:

Examiner:

Attny. Docket No. 068758.0139

Client Ref.: 01003US/RF/SM

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner.

Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

As the Information Disclosure Statement is being submitted before the mailing of the first office action on the merits, Applicants believe that no fee is required. If a fee is

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required, please accept this transmittal as a petition therefor and charge any fee to Baker Botts L.L.P. (formerly, Baker & Botts, L.L.P.) Deposit Account No. 02-0383, Order No. (068758.0139) for any other charges necessary for the filing of this Information Disclosure Statement.

Date: October 31, 2003

BAKER BOTTS L.L.P. (023640)

By: Bruce W. Slayden II

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ATTORNEYS FOR APPLICANTS

Client Reference No. 068758.0139		Application No.	Applicant(s): TED JOHANSSON					
PTO-1449	Information Disclosure Citation in an Application	Docket Number 068758.0139	Group Art Unit	Filing Date October 31, 2003				
U.S. PATENT DOCUMENTS								
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE		
	1	4,622,735	11/18/86	Shibata	29	571	08/29/84	
	2	4,740,484	04/26/88	Norström	437	200	03/04/86	
	3	4,789,995	12/06/88	Hurst et al.	375	75	05/01/87	
	4	5,171,702	12/15/92	Prengle et al.	437	59	10/29/91	
	5	5,374,845	12/20/94	Havemann	257	592	12/02/92	
	6	6,077,752	06/20/00	Norström	438	309	05/19/98	
	7	6,100,133	08/08/00	Norstrom et al.	438	250	10/19/98	
	8	6,198,156	03/06/01	Johansson et al.	257	593	08/28/98	
FOREIGN PATENT DOCUMENTS								
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
						YES	NO	
	9	07335774A	12/22/95	JAPAN (ABSTRACT)	H01L	21/8249	x	
	10	EP 1 094 514 A2	10/17/00	EPO	H01L	21/762	x	
	11	WO98/53489	11/26/98	PCT	H01L	21/331	x	
	12	WO99/03151	01/21/99	PCT	H01L	21/8222	x	
	13	WO01/20664 A1	03/22/01	PCT	H01L	21/76	x	
NON-PATENT DOCUMENTS								
	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)						DATE	
	14	Nandakumar, M, et al. "Shallow Trench Isolation for Advanced ULSI CMOS Technologies"; IEDM Tech. Dig., p. 133						1998
	15	P.C. Hunt, and M.P. Cooke: "Process HE: A Highly Advanced Trench Isolated Bipolar Technology for Analogue and Digital Applications", Proc. IEEE CICC, p. 816						1988
	16	R.D. Rung, et al.: "Deep Trench Isolated CMOS Devices", IEDM Tech. Dig., p. 237						1982
	17	Y.B. Wang, et al.: "Arsenic Enhanced Oxidation and Effective Control of Buried Collector Step" 196th Meeting of The Electrochemical Society (Honolulu, Hawaii)						10/17-22/1999
	18	G. Niu et al.: "Intermodulation Characteristics of UHV/CVD SiGe HBT's"; Proceedings of the IEEE BCTM Conference, p. 50-53						1999
	19	S. Wolf, "Silicon Processing for the VLSI Era, Volume 2 - Process Integration", Lattice Press, Sunset Beach						1990
EXAMINER				/H Tsai/ (06/25/2008)		DATE CONSIDERED		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.								